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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/629,069

07/29/2003

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EXAMINER

ABRAHAM, FETSUM

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/629,069

Applicant(s)

YAMAZAKI ET AL.

Examiner

Fetsum Abraham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 36-42 and 51-63 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) all is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Claims rejection

As a preliminary matter, please notice the withdrawal of the previously indicated allowable subject matter in view of the newly found primary reference.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 36,51,58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aomori et al (5,504,020).

The prior art discloses a TFT structure having a gate formed on active SOI layer as follows:

Detailed Description Text (73):

In this invention, the gate electrode can be made of a material selected from a group including aluminum, a metal containing aluminum, and a layered structure of aluminum and a metal other than aluminum. Alternatively, the gate electrode can be made of a material from a heavy metal such as Pt and Au or a silicide such as tungsten silicide and titanium silicide. In such a case, the wiring resistance of the gate electrode is lowered and also a high stop ability against the ion shower doping can be attained by a thin film thickness.

Clearly, the claimed material is one of the gate materials selected in the prior art. Metal other than aluminum implies tungsten from broader sense of interpretation. Tungsten silicide also comprises tungsten as a major part of the material.

Further, the prior art teaches the following on how the active layers of the TFT were made:

Brief Summary Text (33):

In addition, the resist pattern used for forming the gate electrode of the TFT is used as a mask for impurity implantation, so that the photolithography process for forming a mask can be omitted. This mask can also protect the gate electrode from the impurity elements and hydrogen.

"This mask can also protect the gate electrode from the impurity elements and hydrogen" implies that the mask stays on the gate during its usage in the process of forming the active layers considering the fact that the source and drain regions of the TFTs are positioned at the outer ends of the gates of the gates of the same. Besides, claim 1 of the patent asserts that the active layers were formed by using the mask that formed the gates and the gate as a composite mask.

The prior art discloses all subject matter claimed but may have been silent on using the TFT in display structure having a pixel. However, TFTs with gate insulation materials are the generic display switches in the art. Therefore, it would have been obvious to one skilled in the art to use the prior art TFT in display devices in contact with a pixel and repeat the structure to make it applicable in the entire display matrix since display matrices are designed to use TFTs as switching elements.

As for the driving circuit in claim 39, all display structures have drivers associated with for proper functionality.

Claims 37,38,39,41,42,52-54,56,57,59,60,61,63,64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aomori et al (5,504,020) in view of Takayama et al (6,661,096).

As for claims 37,39,41,52,54,56,57,59,60,61,63,64, the primary art teaches all subject matter claimed but may have omitted a laminated gate structure composed of tungsten and tungsten nitride formed by nitridation method. However, the secondary reference teaches the missing element as presented below:

Detailed Description Text (79):

The gate wirings of the TFTs 1801 to 1804 shown in FIG. 18 are lamination structures of the tungsten nitride film 1702 and the tungsten film 1703. By using the sputtering method shown in the embodiment mode, the amount of sodium contained in the gate wirings can be made equal to or less than 0.3 ppm, preferably equal to or less than 0.1 ppm, the concentration of oxygen within the wirings can be made equal to or less than 1 wt %, preferably equal to or less than 0.2 wt %, and the electrical resistivity of the wirings can be made from 6 to 15 $\mu\Omega\cdot\text{cm}$. Further, the film stress can be controlled within the range of -1×10^{10} dyn/cm² to 1×10^{10} dyn/cm².

Therefore, it would have been obvious to one skilled in the art to laminate the primary gate with tungsten nitride film because such films serve the gates as barrier materials from diffusion induced contamination by other materials positioned adjacent to the gates.

As for claims 38,42,53,57,60,64 sputtering is a common method of making gate structures. Sputtering is the most basic method of depositing a metal layer on silicon based layers and would have been obvious to one skilled in the art to use it in the

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making of the gate layer of the prior art since it has a better focusing feature on a target than vacuum evaporation based processes.

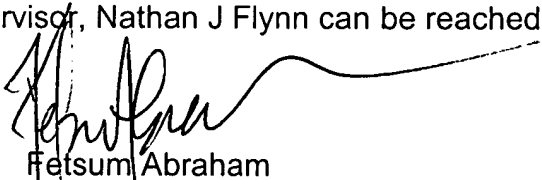
Further, as for the driving circuit in claims 39,54, all display structures have drivers associated with for proper functionality.

Claims 40,55,62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aya et al (6,281,057) in view of Takayama et al (6,661,096) and further in view of Ono et al (5,422,209).

The first two references may have been silent on nitride interlayer on semiconductor structures formed by the claimed process. However, Ono et al teach on interlayer structures made from a nitride film by plasma CVD processing means. Therefore, it would have been obvious to use nitrides made by the taught process, since the prior art teach that such materials provide excellent adhesion and formability compared to other conventional materials such as amorphous nitrides and oxides (see column 8, 60-65).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.



Fetsum Abraham

3/7/06